GSM TELEPHONE
SGH-C200

SERVICE Manual

GSM TELEPHONE



CONTENTS

ELECTRONICS

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BASIC.

1. SGH-C200 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880
ARFCN range	1~124	0~124 & 975~1023	512~885
Tx/Rx spacing	45MHz	45MHz	95MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	35Km	2Km

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2. GSM TX power class

TX Power control level	GSM900
5	33±2 dBm
6	31±2 dBm
7	29±2 dBm
8	27±2 dBm
9	25±2 dBm
10	23±2 dBm
11	21±2 dBm
12	19±2 dBm
13	17±2 dBm
14	15±2 dBm
15	13±2 dBm
16	11±3 dBm
17	9±3dBm
18	7±3 dBm
19	5±3 dBm

TX Power control level	DCS1800
0	30±2 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

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2. SGH-C200 Circuit Description

1. SGH-C200 RF Circuit Description

1) RX PART

1. ASM(U1007) → Switching Tx, Rx path for EGSM900, and DCS1800 by logic controlling.

2. ASM Control Logic (U1007) → Truth Table

	VC1	VC2
DCS / PCS Tx Mode	H	L
GSM Tx Mode	L	H
GSM / DCS Rx Mode	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (C905,L903) → For filtering the frequency band between 925 ~ 960 MHz
- DCS FILTER (C919,L907) → For filtering the frequency band 1805 ~ 1880 MHz.

4. TC-VCXO (OSC900)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U900 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. SI4206 (U900)

This chip integrates two differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from frequency synthesizer. The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

Also, this chip down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

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2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U900 chip.
SI4206 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U100).
The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc

2. Baseband Circuit description of SGH-C200

1) CSP2200B1

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity. A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the CSP2200B1 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register. Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps.

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Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

4. Vibrator Motor Driver

The vibrator motor driver is a independent voltage regulator to drive a small dc motor that silently alerts the user of an incoming call. The driver is a 3.0V constant source while sinking up to 180mA and controlled by enable signal of main chip. For efficient use and safety, the vibrator motor should be connected between the regulator output and the ground.

2) Connector

1. LCD Connector

LCD is consisted of main LCD(color 65K STN LCD). Chip select signals of EMI part in the trident, LCD_CS, can enable main LCD. LED+ signal enables white LED of main LCD. In sleep mode, white LED are turned off.
These two signals are from IO part of the DSP in the trident. RST signal from CSP2200B1 initiates the initial process of the LCD.
16-bit data lines(D(0)~D(15)) transfers data and commands to LCD through emi_filter. Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data.
The signals which inform the input or output state to LCD, are required. But this system is not necessary for read enable signal. CP_WEN signal is only used to write data or commands to LCD.
Power signal for operating LCD driver is VCCD.

2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.
CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

3. Keypad connector

This is consisted of key interface pins in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix.
So power on/off signal is connected with CSP2200 to enable CSP2200.
Nine key LED use the +VBATT supply voltage. These are connected to BACKLIGHT signal in the CSP2200.
This signal enables LEDs with current control.

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4. EMI Filtering

This system uses the EMI Filter to reduce noise from LCD part. Some control signals are connected to LCD without EMI filtering.

3) IF connetor

It is 24-pin connector, and separated into two parts. One is a power supply part for main system. And the other is designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, and GND. They connected to power supply IC, microprocessor and signal processor IC.

4) Audio

AOUTAP, AOUTAN from CSP2200 is connected to the speaker via analog switch. AOUTBP and AOUTBN are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.
YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU762MA3 is equipped 16 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.
YMU762 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.
For the headphone, it is provided with a stereophonic output terminal.
For the purpose of enabling YMU762MA3 to demonstrate its full capabilities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

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5) Memory

This system uses FUJITSU's memory, MB84VP24491HK.
It is consisted of 128M bits flash memory and 32M bits FCRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP2200. It has 22 bit address lines, A[1~22]. They are also connected. CP_CSROMEN signal, chip select signal in the trident, enable flash memories. They use 3 volt supply voltage, VCCD.
During wrting process, CP_WEN is low and it enables writing process to flash memory and FCRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or FCRAM to data lines. Each chip select signals in the trident select flash memory or SCRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from CSP2200, for ESD protection. A[0] signal enables lower byte of FCRAM and UPPER_BYTE signal enables higher byte of FCRAM.

6) Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface.
DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP2200. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762.
ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.
CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.
Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communications using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).
And UP_CS/SCLK/SDI, control signals for CSP2200 are outputted through PPI pins. It has signal port for charging(CHG_DET), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

7) CSP2200

CSP2200 is integrated the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions, and power management block. The CSP2200 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP2200's internal register, and program CSP2200's event timing and control register with the exact time to send the

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burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP2200's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP2200 then notifies the DSP which has sample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

There are 7 LDOs which are power sources of microprocessor, LCD, etc. These 7 LDOs output are programmable.

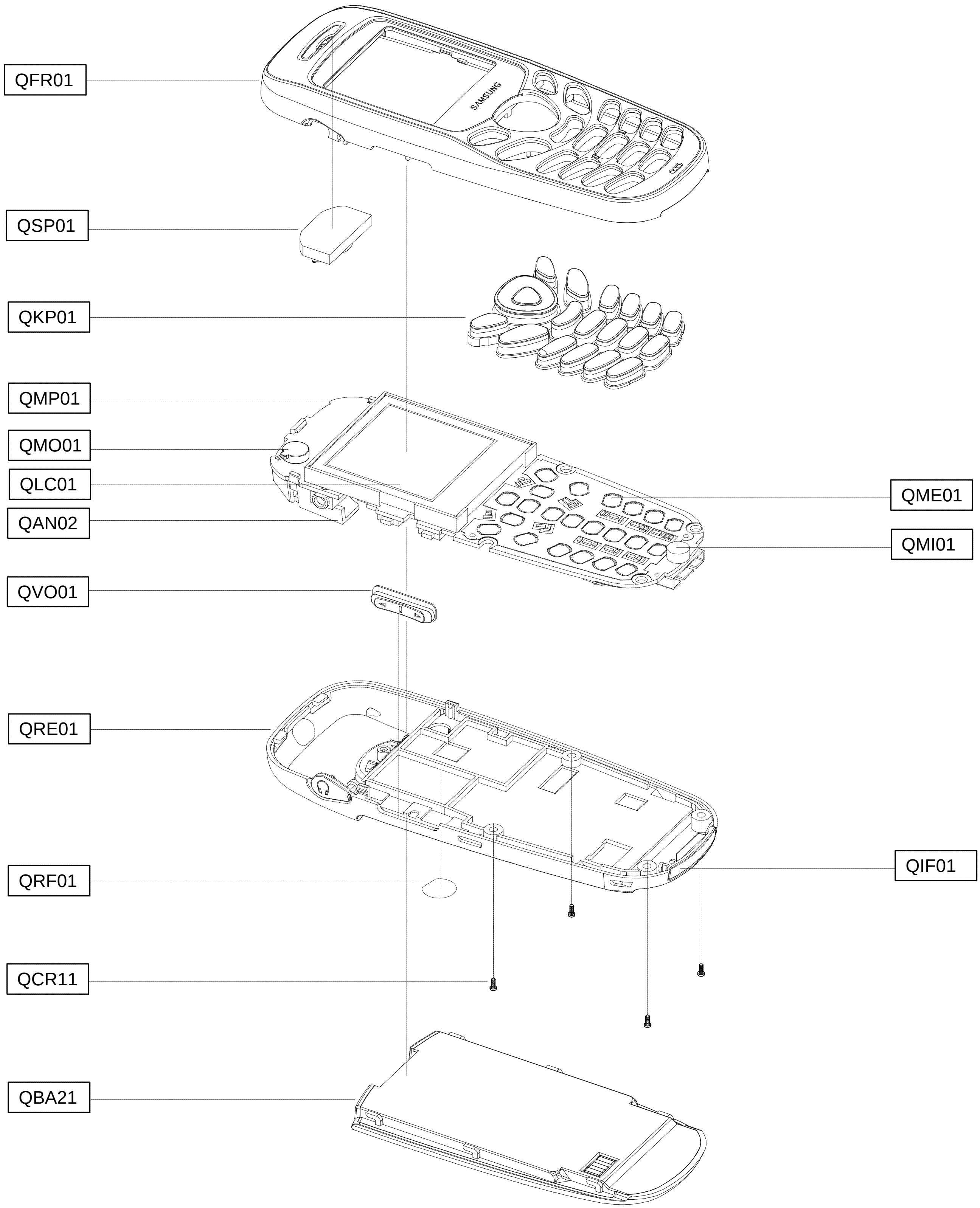
8) X-TAL(13MHz)

This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is fed to CSP1093,Trident,YMU762 and Silab solution.

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3. SGH-C200 Exploded View and its Parts list

1. Cellular phone Exploded View-1



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2. Cellular phone Parts list

Location NO.		Description	SEC CODE	Remark
QFR01		FRONT COVER	GH75-04852B	
QKP01		KEYPAD	GH75-04858A	
QMP01		MAIN PBA	GH92-01791A	
QLC01		LCD	GH07-00555A	
QAN02		INTENNA	GH42-00416A	
QRE01		REAR COVER	GH75-04854B	
QME01		METAL DOME	GH59-01457A	
QMI01		MICROPHONE	GH30-00112A	
QIF01		IF COVER	GH72-14172B	
QVO01		SIDE KEY	GH75-04859A	
QCR11		SCREW	6001-001654	
QBA21		BATTERY	GH43-01356B	
QSP01		SPEAKER	3001-001568	
QRF01		RF SHEET	GH74-08818B	
QMO01		MOTOR	GH31-00103A	

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3. Test Jig (GH80-00865A)



3-1. RF Test Cable (GH39-00182A)



3-2. Test Cable (GH39-00127A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE (GH39-00143B)



3-6. TA (GH44-00482A)



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4. SGH-C200 MAIN Electrical Parts List

SEC Code	Design LOC
0403-001387	ZD302
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0403-001427	ZD303
0406-001083	ZD300
0406-001083	ZD301
0406-001194	ZD803
0406-001201	ZD408
0406-001201	ZD407
0406-001201	ZD406
0406-001201	ZD405
0406-001201	ZD404
0406-001201	ZD403
0406-001201	ZD402
0504-000168	Q100
0601-001795	D801
0601-001795	D802
0601-001795	D803
0601-001795	D804
0601-001795	D805
0601-001795	D806
0601-001795	D807
0601-001795	D808
0601-001795	D809
0601-001795	D811
0801-000796	U102
1001-001294	U402
1109-001302	U500
1201-002174	U1000
1201-002176	U404
1203-002168	U403
1203-003105	U801
1203-003304	U100
1203-003389	U101
1203-003443	U200
1204-002161	U401
1205-002485	U900
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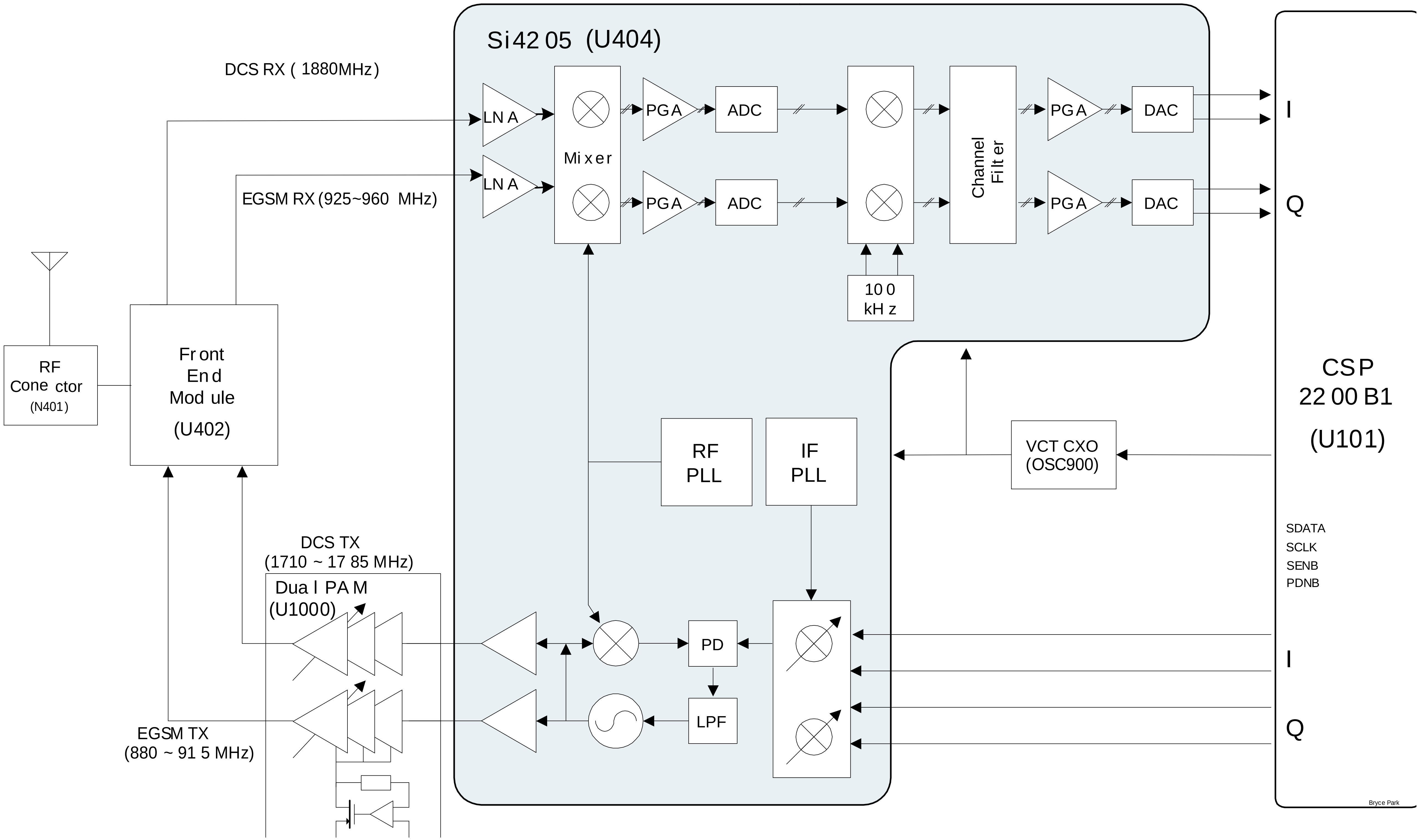
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2404-001105	C412
2404-001105	C436
2404-001105	C437
2404-001134	C1003
2404-001240	C109
2404-001268	C124
2404-001268	C125
2404-001268	C303
2404-001268	C408
2404-001305	C426
2503-001041	C220

SEC Code	Design LOC
2503-001041	C221
2703-002170	L907
2703-002199	L903
2703-002202	L401
2703-002202	L402
2703-002204	C1007
2703-002204	L1007
2703-002205	L900
2703-002267	C1005
2703-002339	L201
2703-002367	L1005
2703-002558	L902
2703-002636	L906
2801-003856	OSC600
2801-004359	OSC900
2901-001286	F204
2901-001286	F203
2901-001286	F202
2901-001286	F201
2901-001286	F200
2904-001523	F100
2909-001216	U1007
3301-001659	L301
3404-001152	VOL_DN
3404-001152	VOL_UP
3705-001287	CON1
3709-001229	CN100
3710-001611	CN300
3711-005558	CN301
3722-002067	CN401
4302-001130	C108
GH09-00029A	U600
GH41-00610A	

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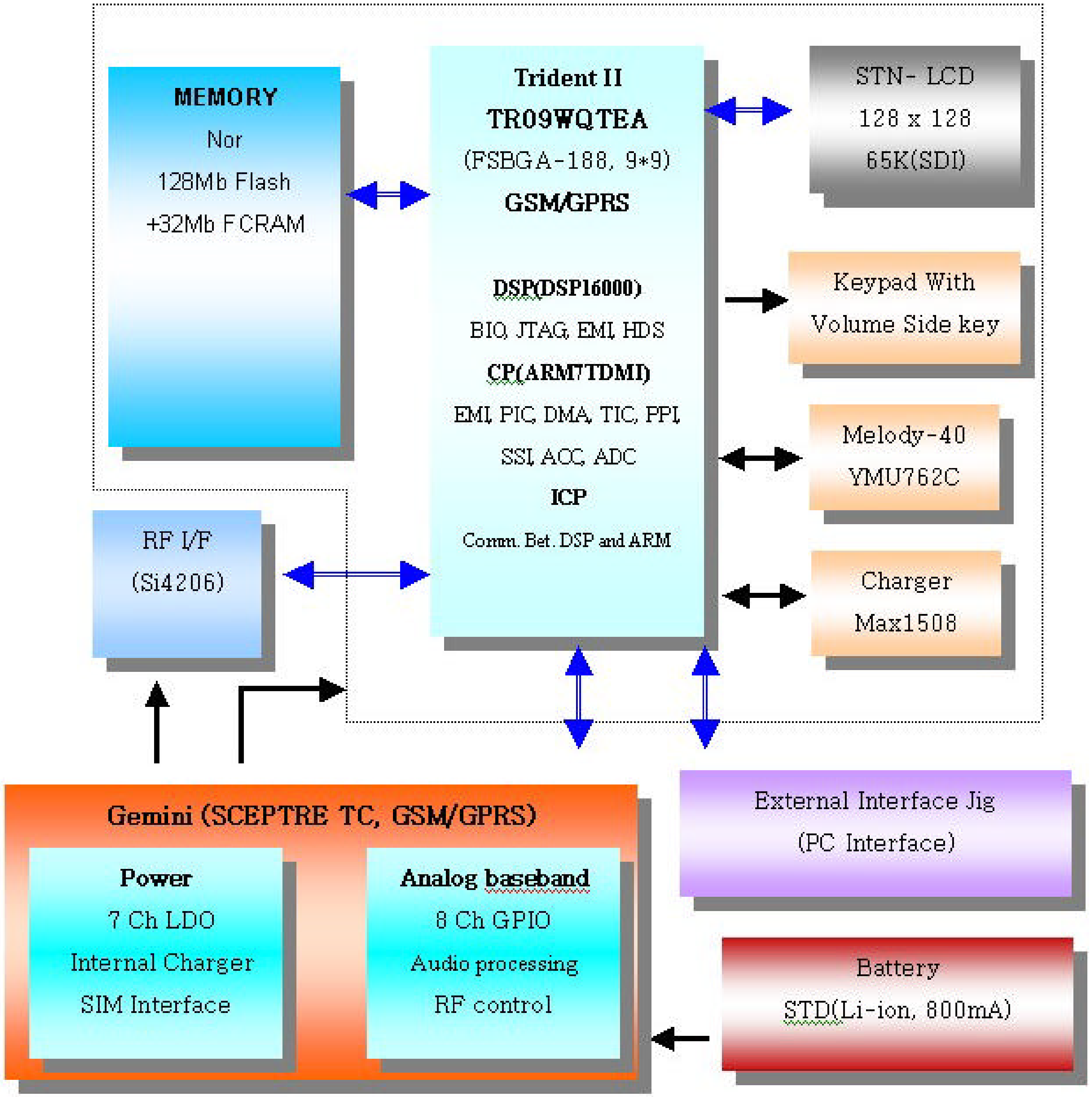
5. SGH-C200 Block Diagrams

1. RF Solution Block Diagram



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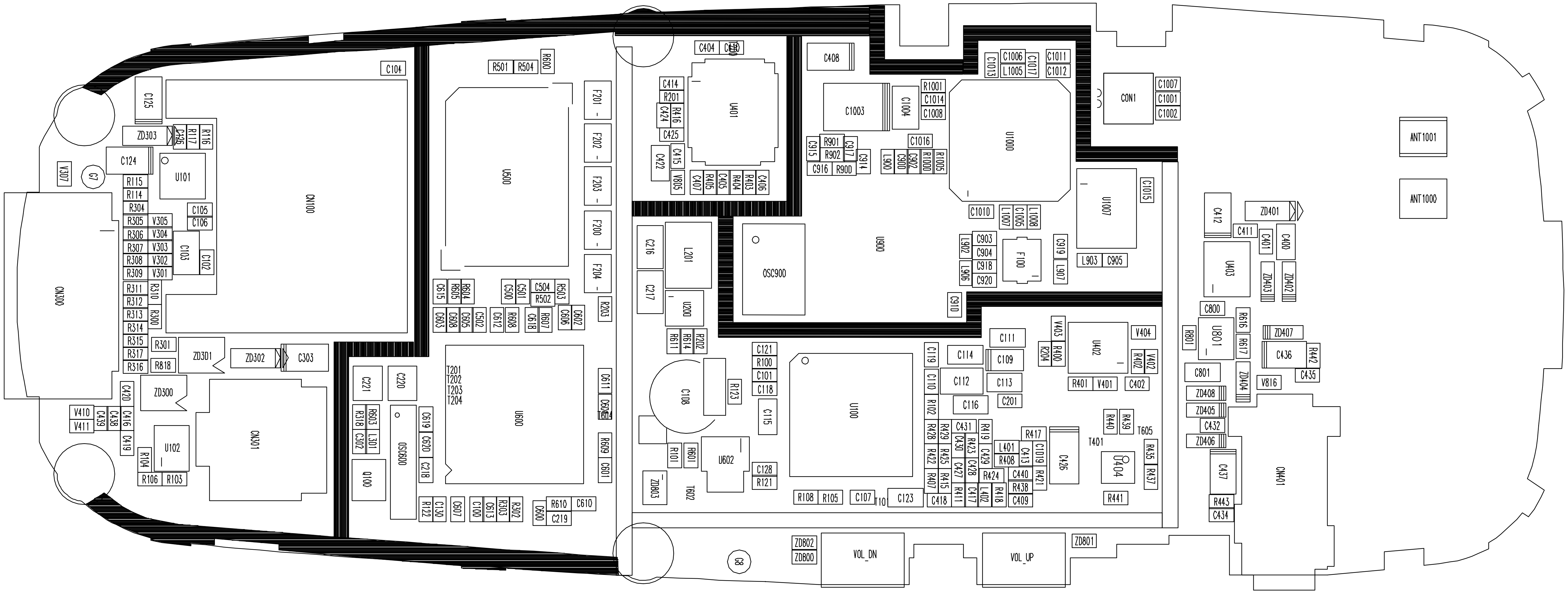
2. Base Band Solution Block Diagram



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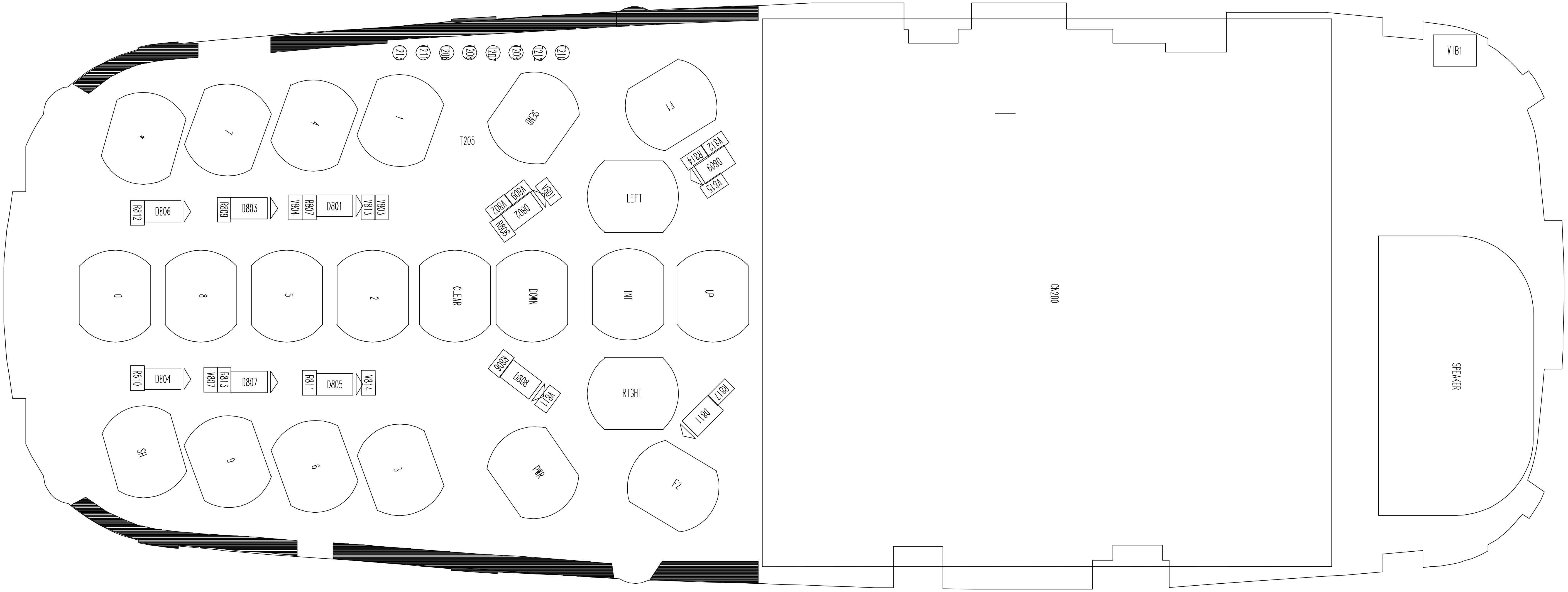
6. SGH-C200 PCB Diagrams

1. Main PCB Top Diagram



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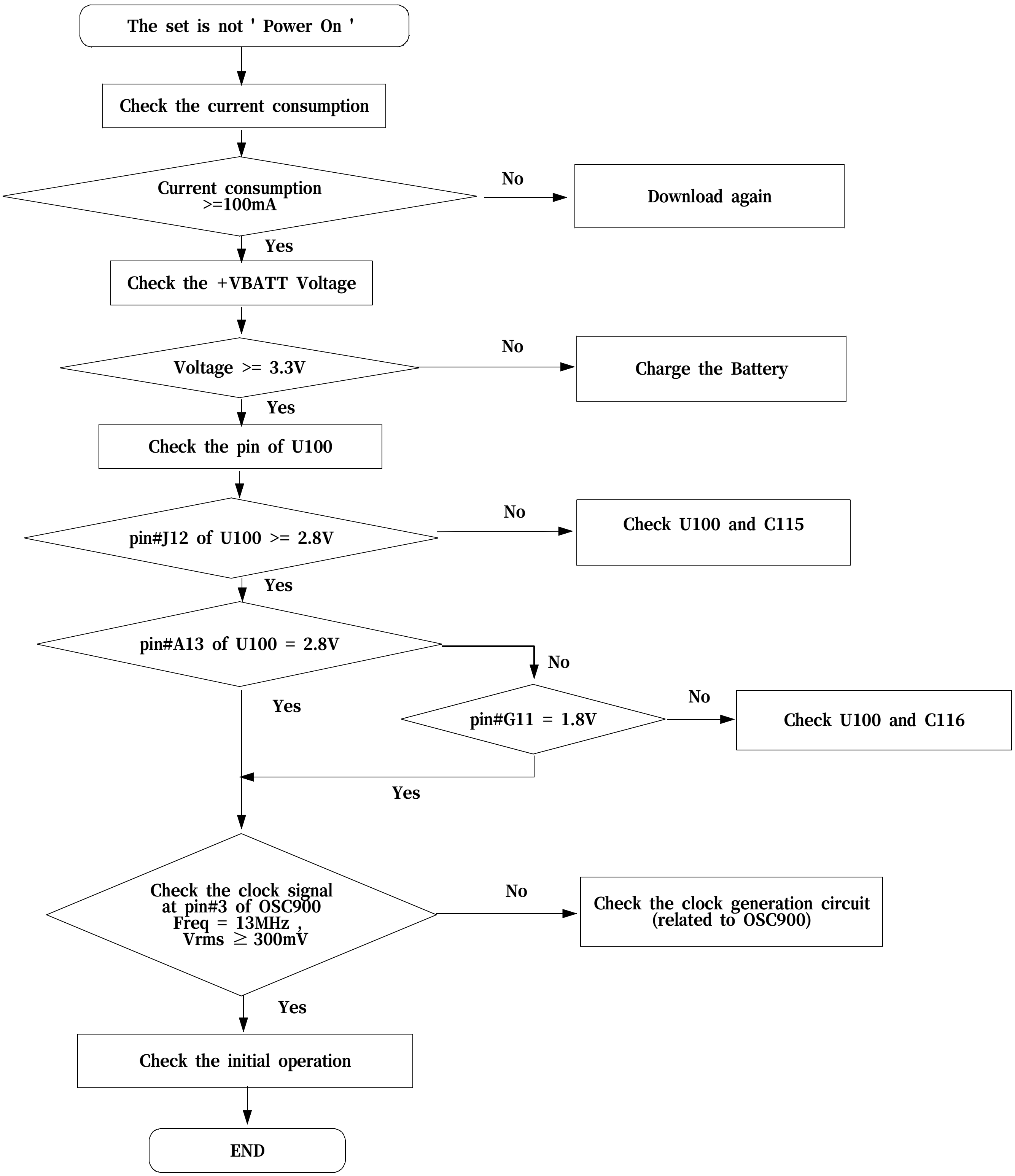
2. Main PCB Bottom Diagram



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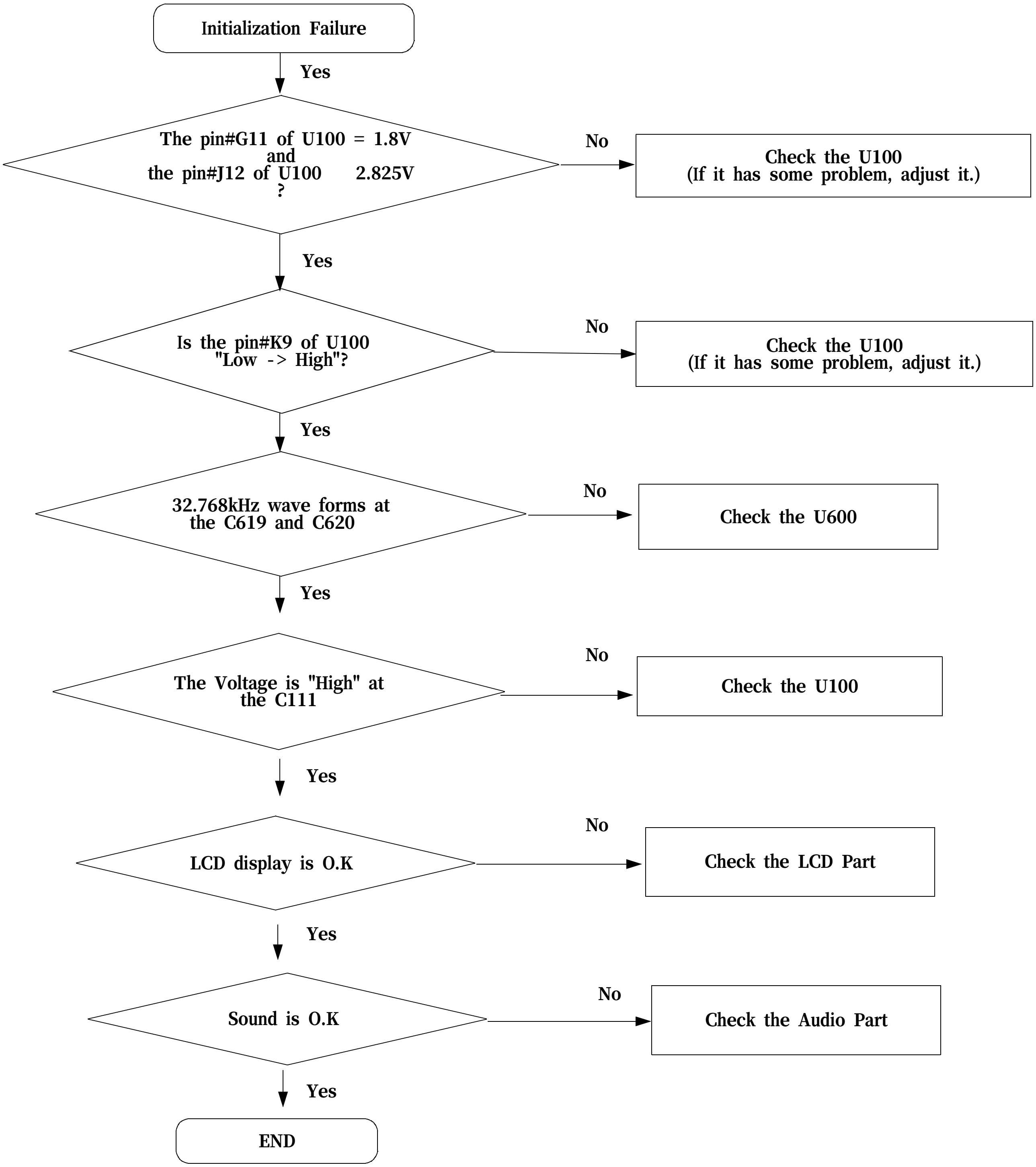
7. SGH-C200 Flow Chart of Troubleshooting

1. Power On



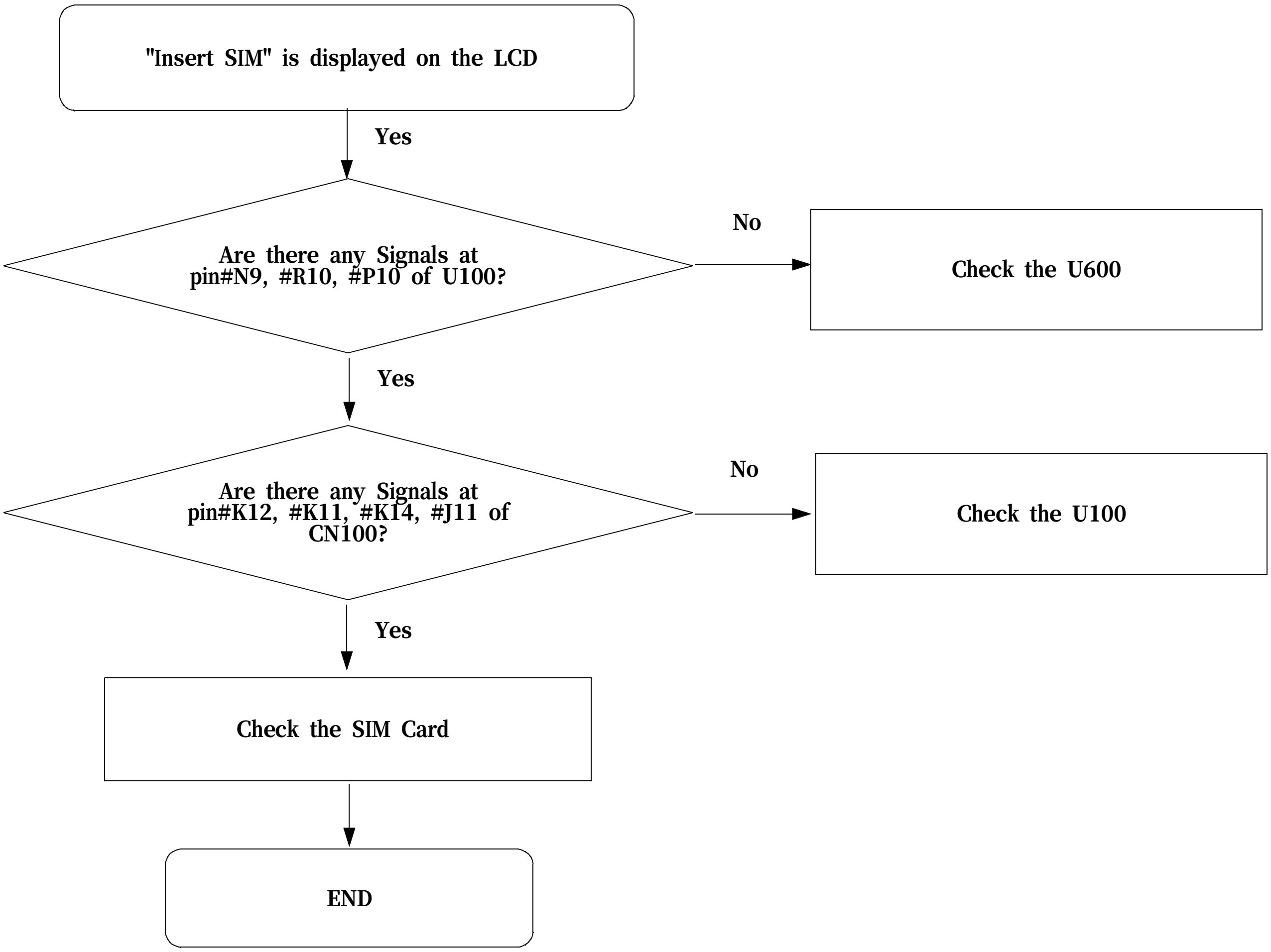
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2. Initial



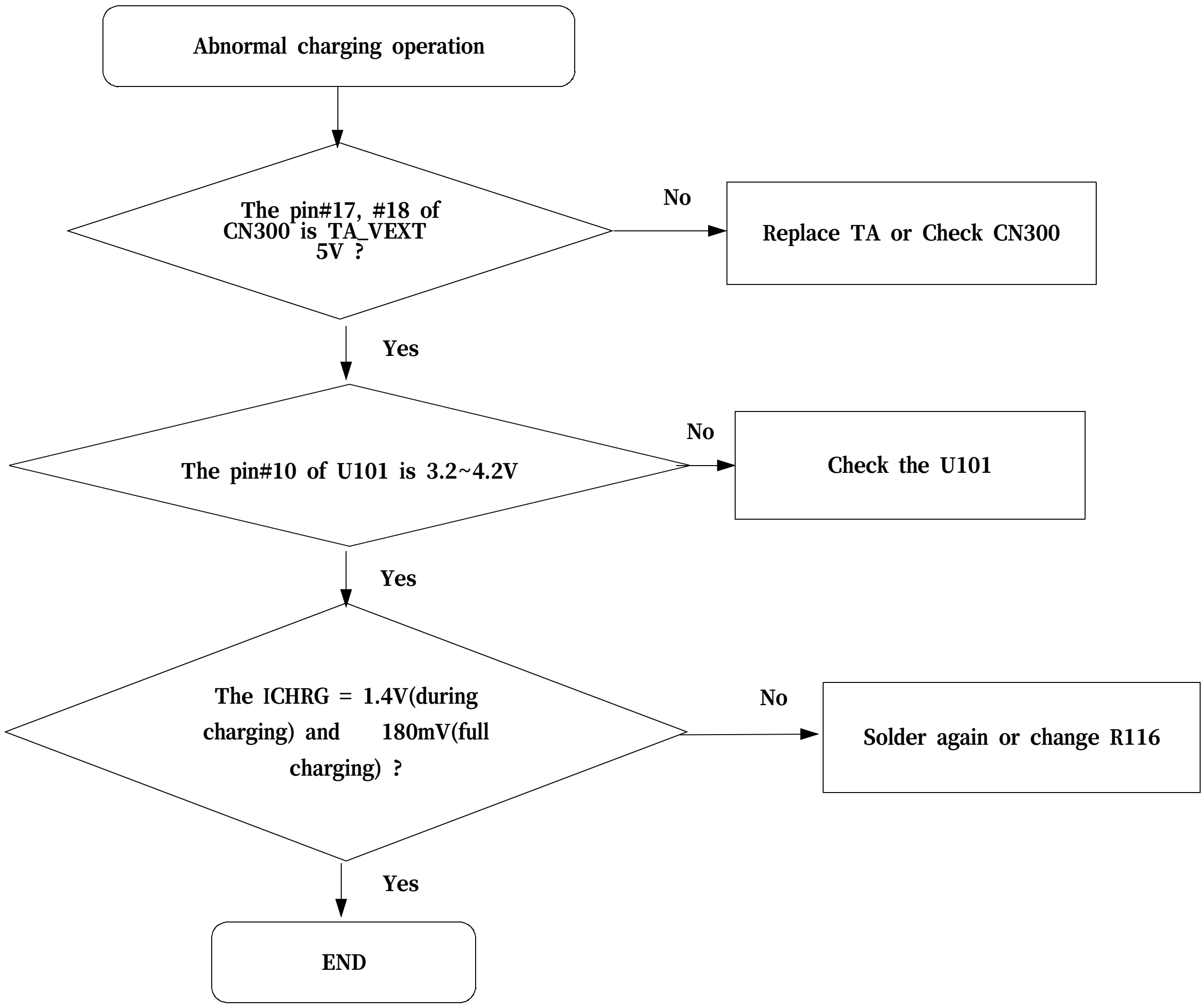
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3. SIM Part

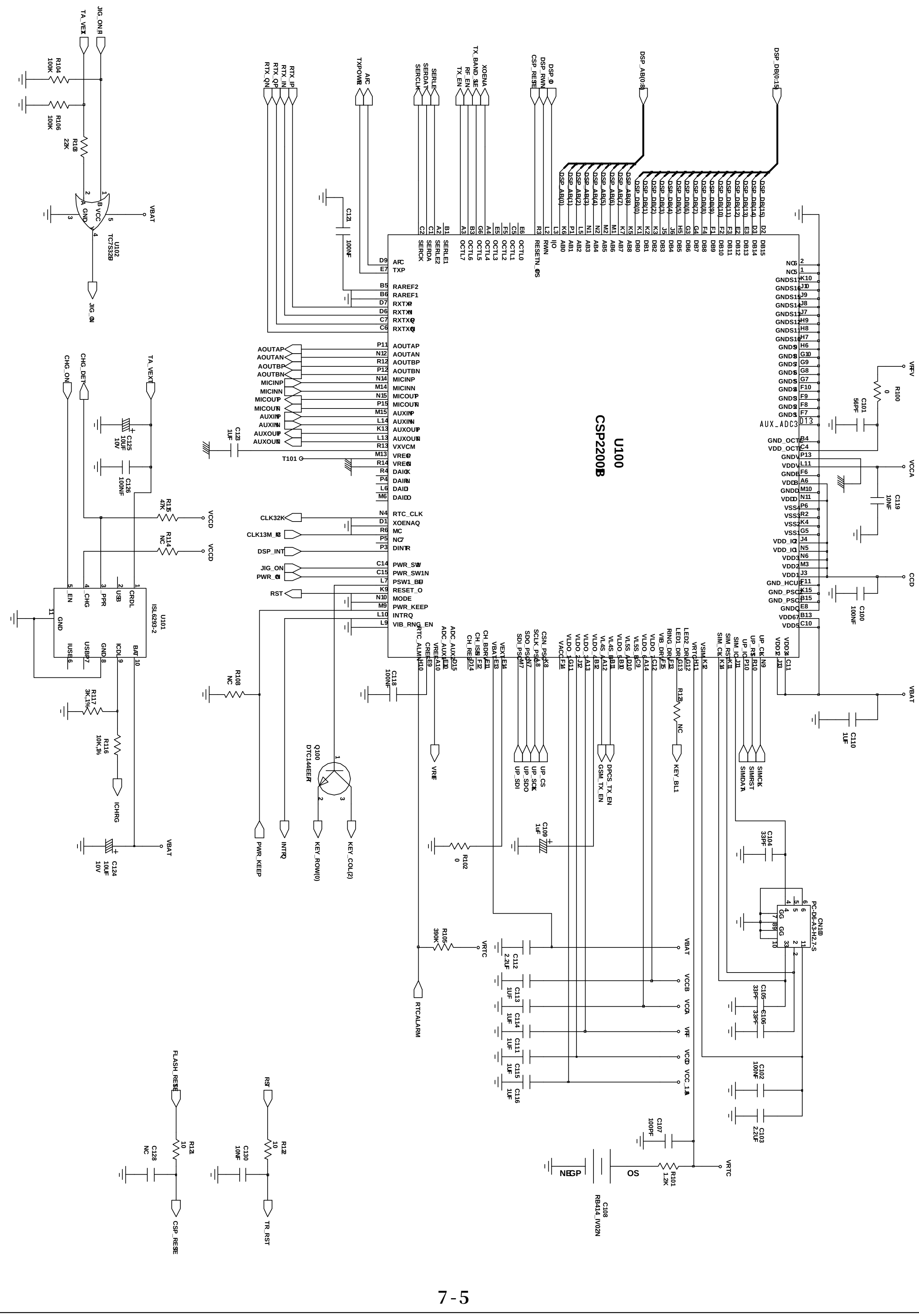


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4. Charging Part

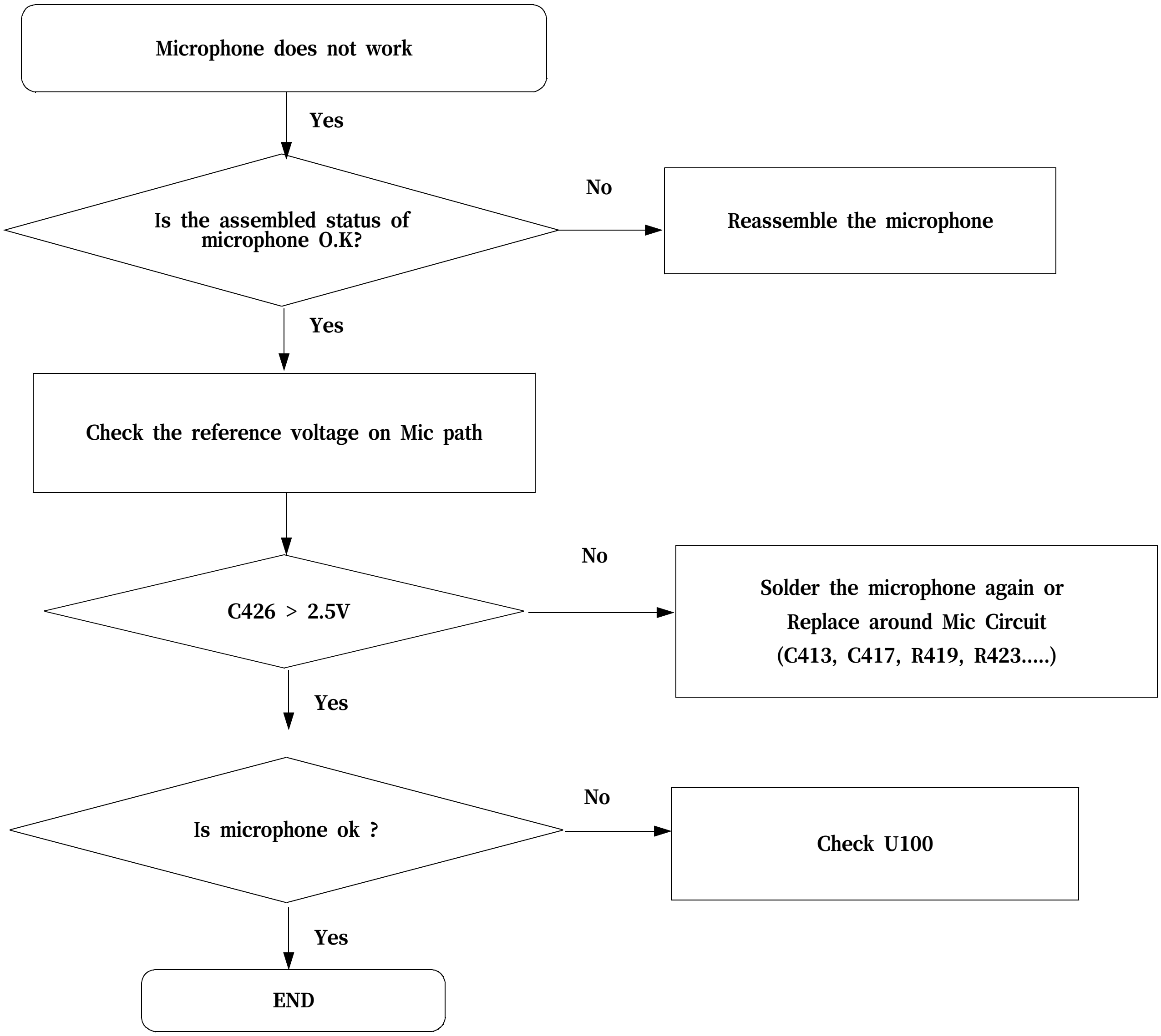


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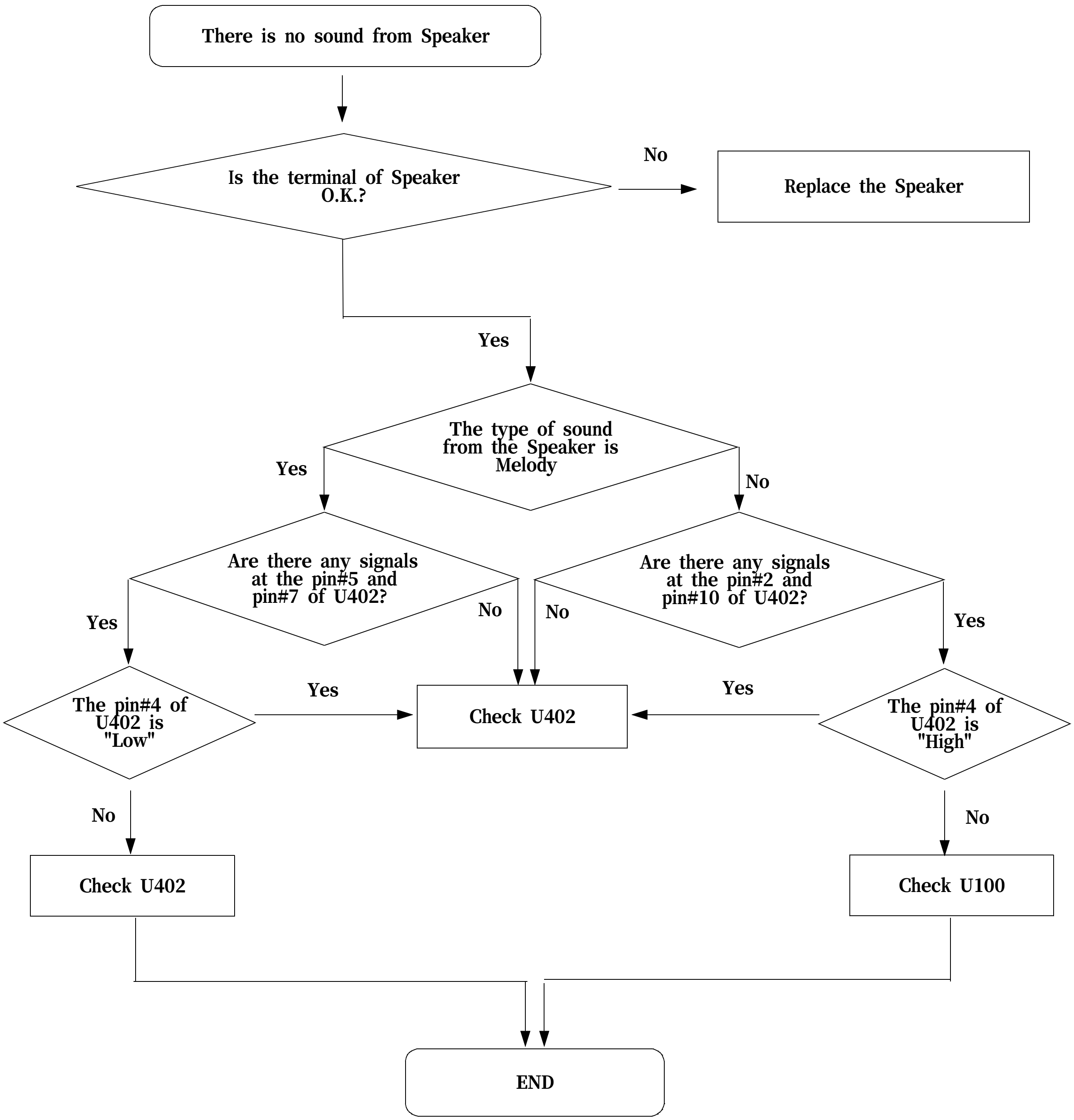
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5. Microphone Part

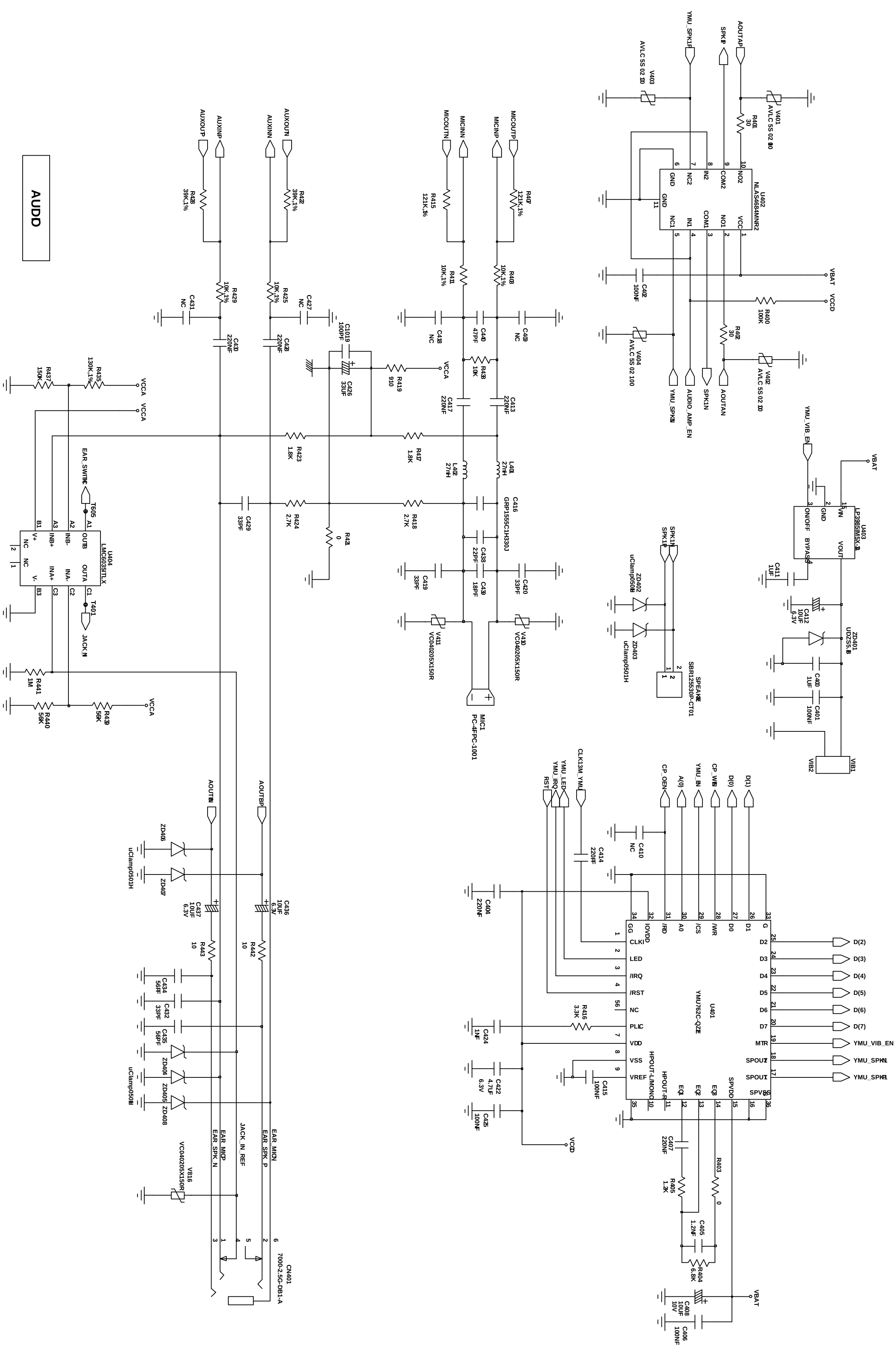


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6. Speaker Part

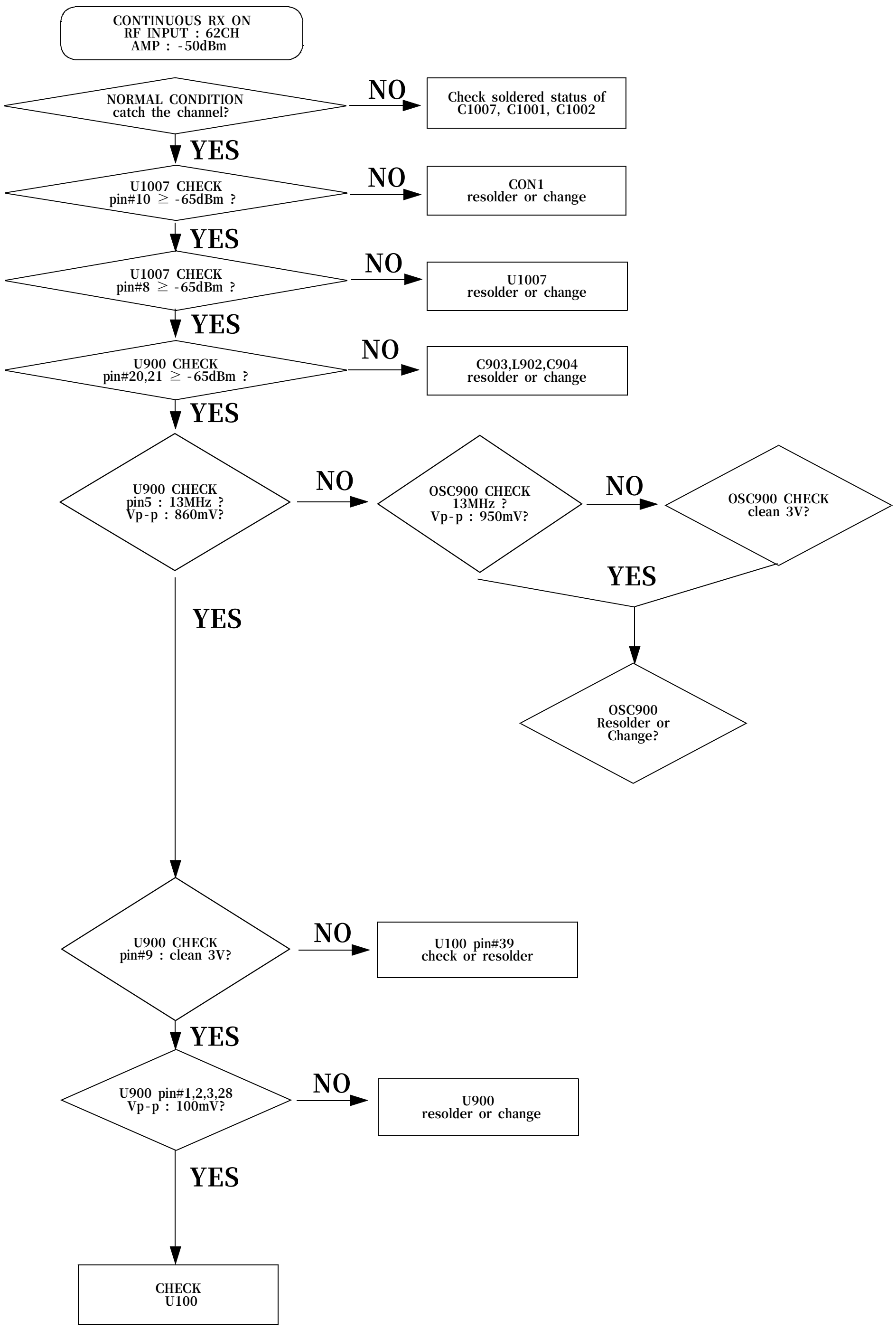


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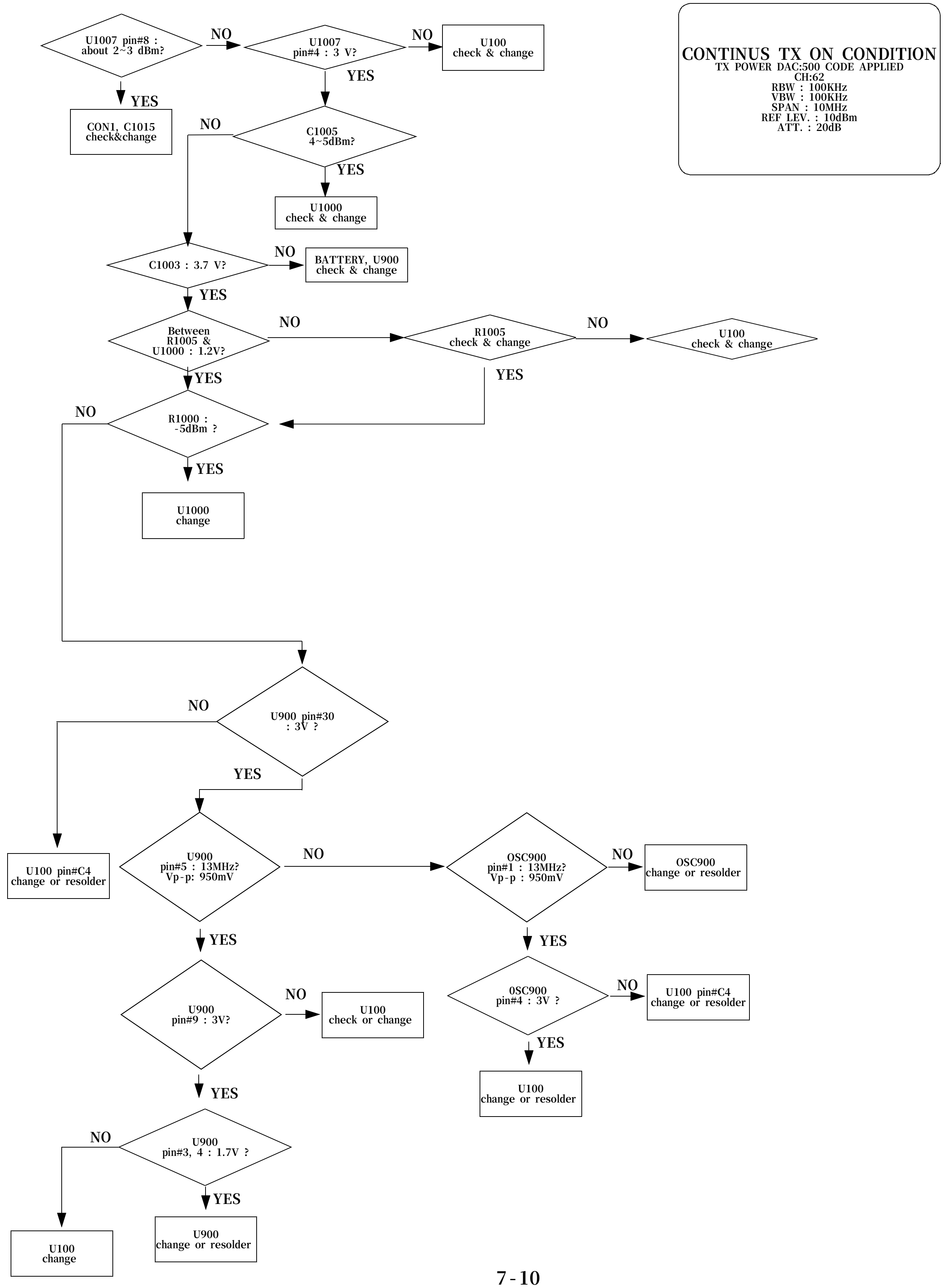
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8. EGSM Reciever



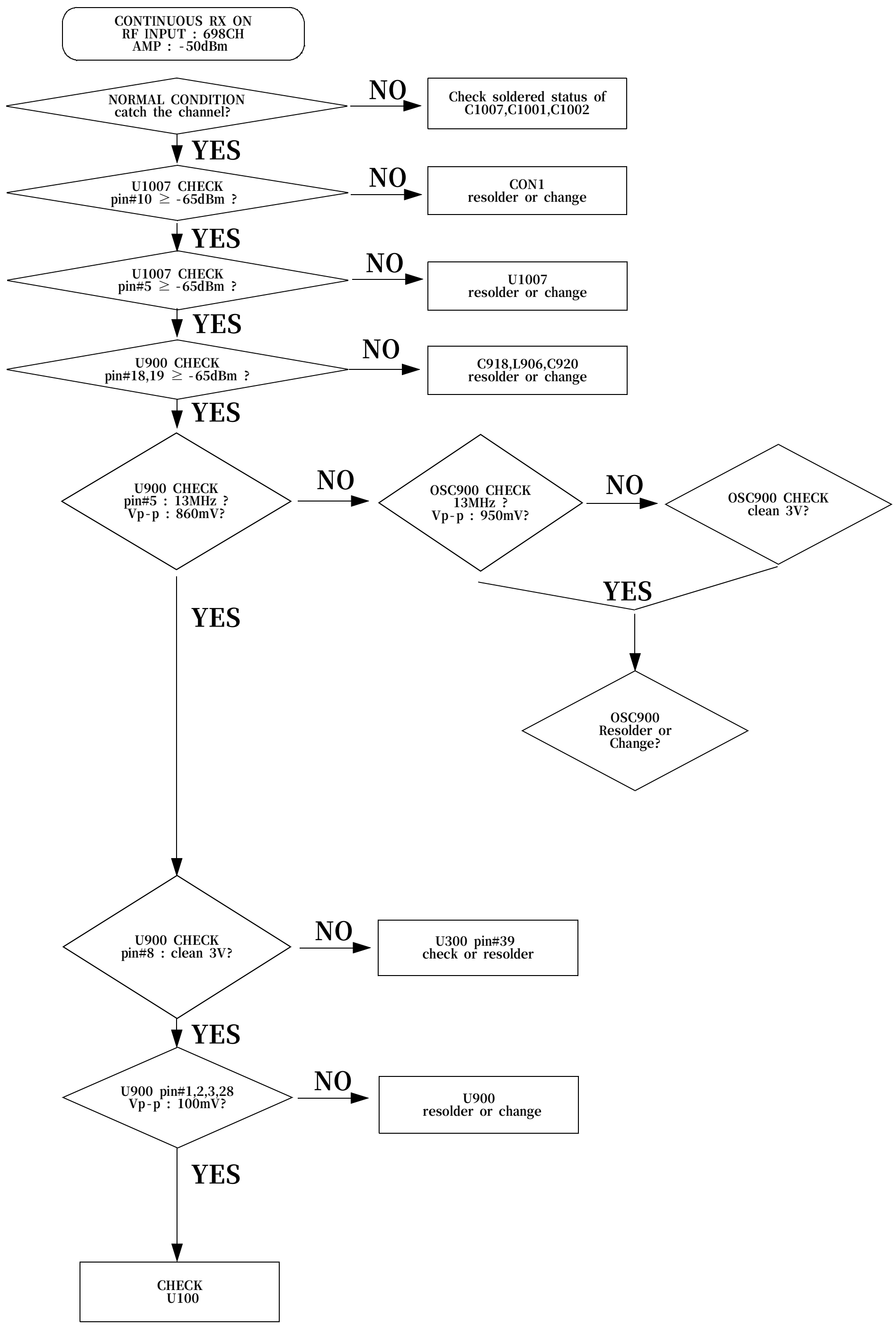
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9. EGSM transmitter



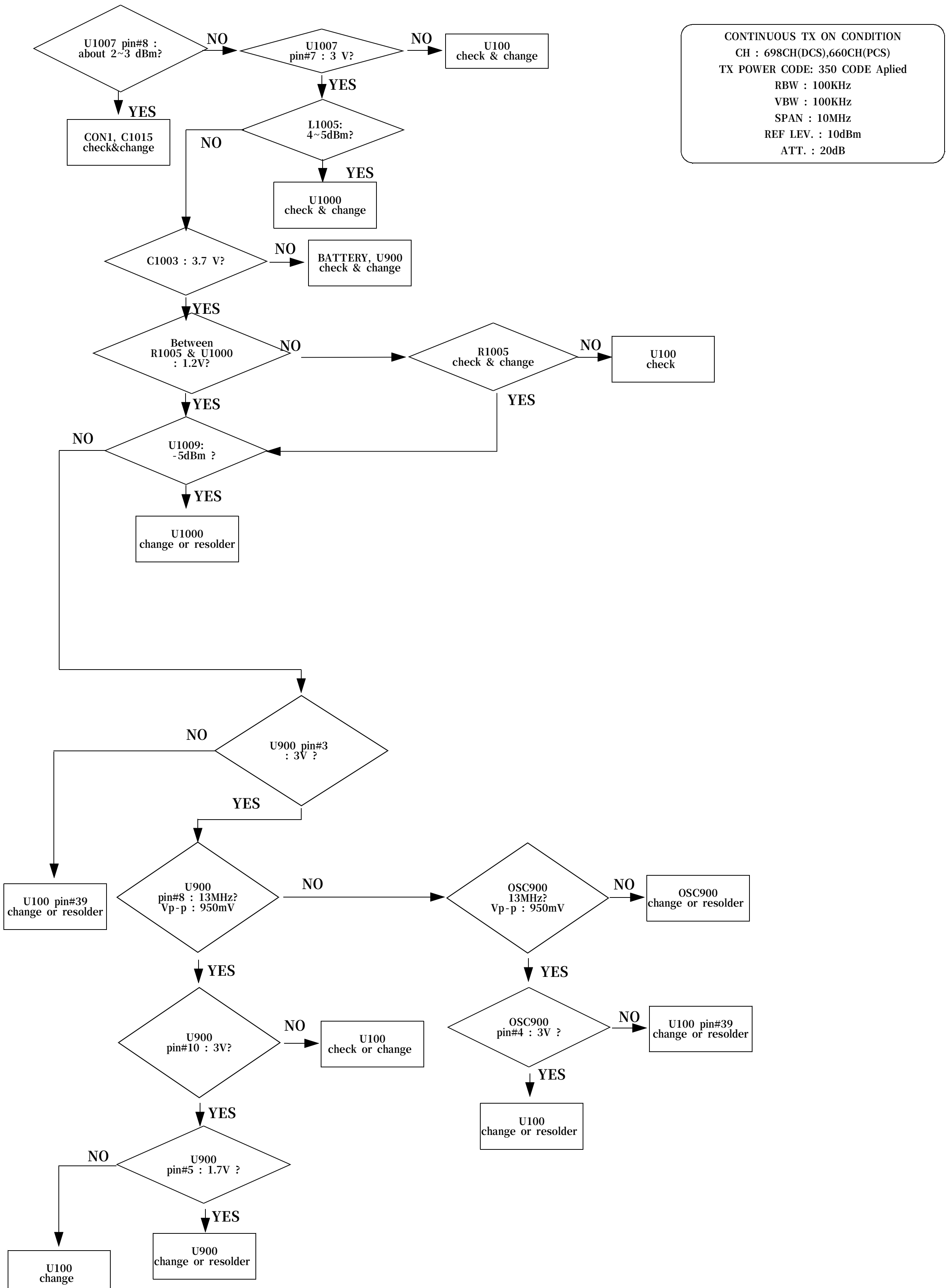
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10. DCS Receiver

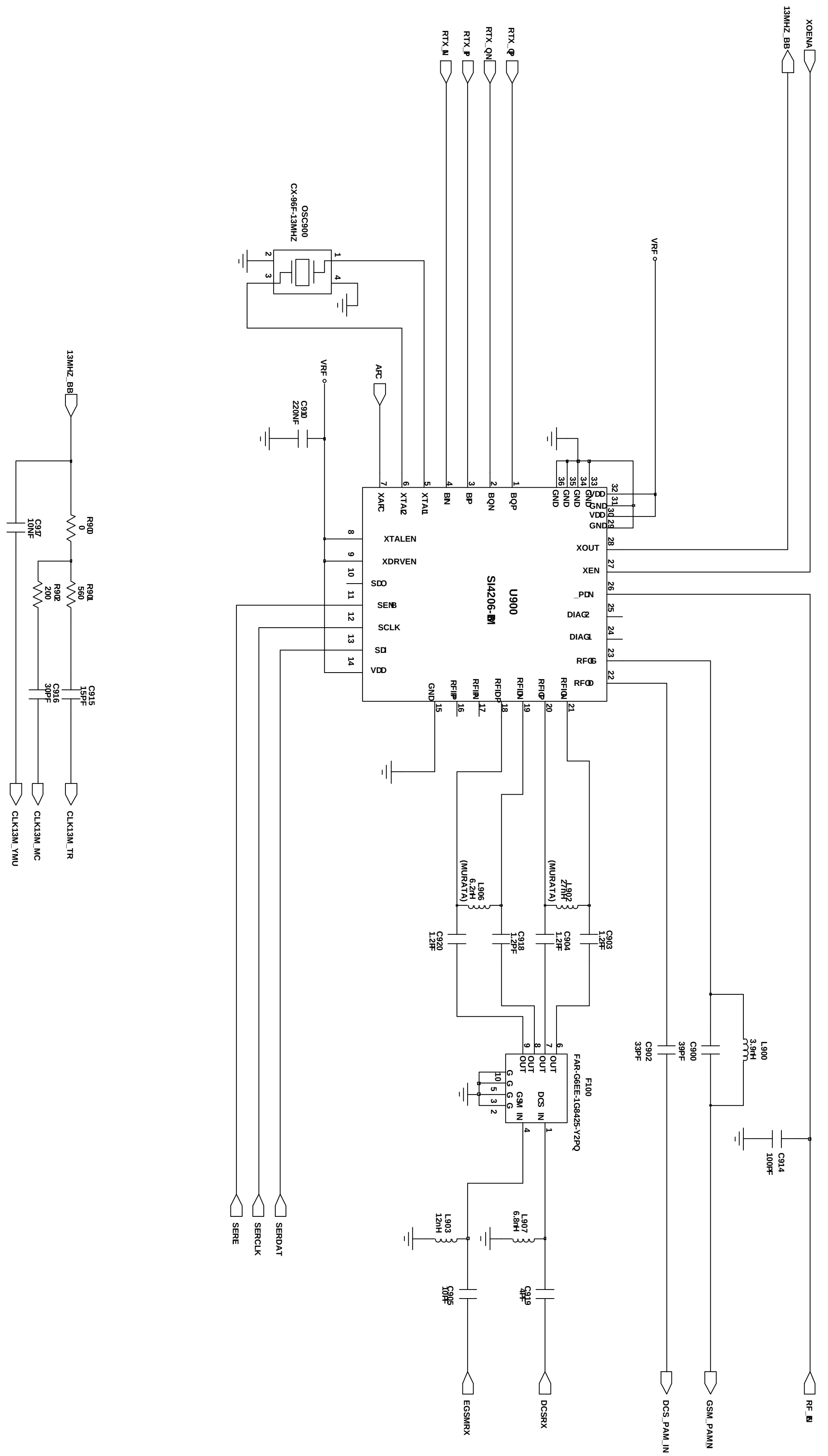


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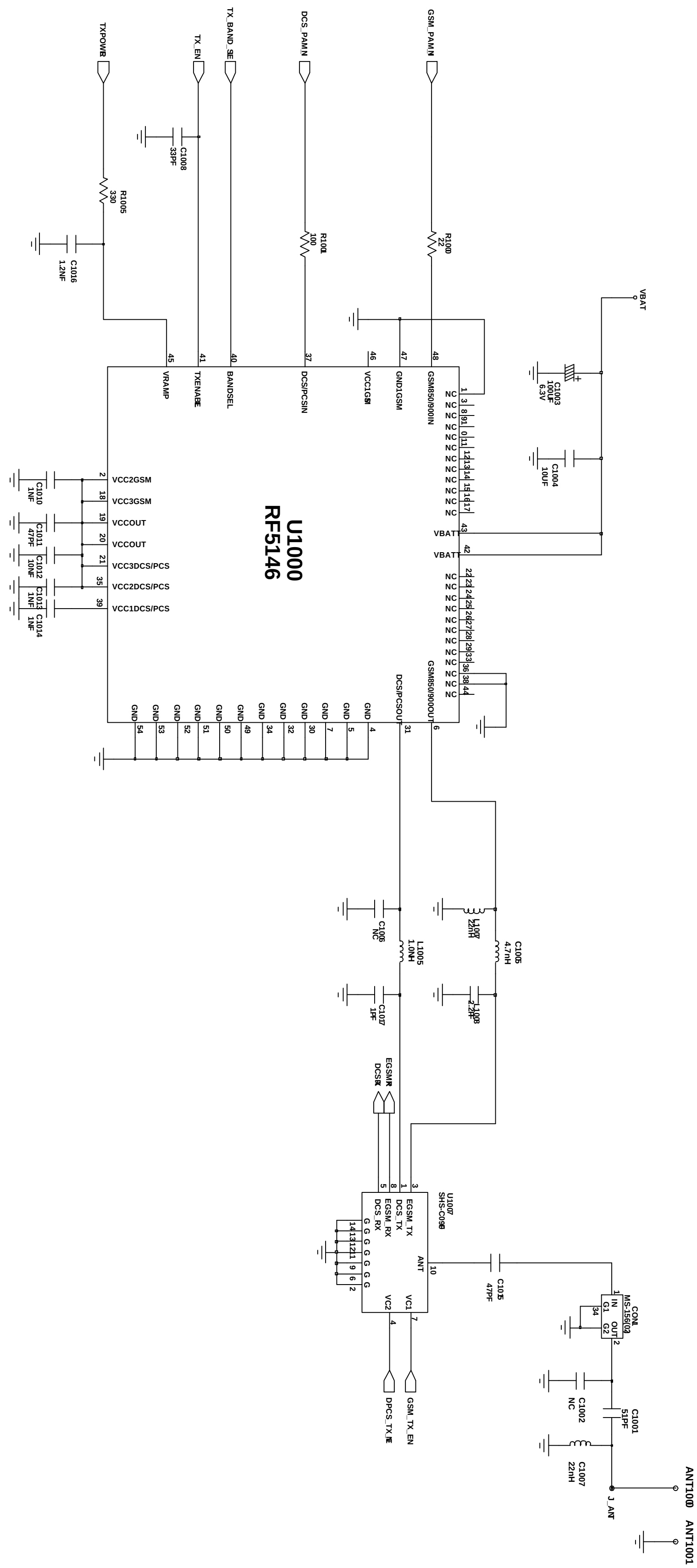
11. DCS transmitter



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